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Design of Testable Reversible ALU using QCA Multiplexer

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Abstract: International Technology Roadmap for Semiconductors (ITRS) has indicated several new technologies alternative for CMOS nanotechnology, some of these include Resonant Tunneling Diodes (RTDs), Single Electron Tunneling (SET), Quantum Cellular Automata (QCA), and Tunneling Phase Logic (TPL). Among these, QCA seems to be the most promising emerging technology, as a viable alternative to CMOS. ALU is a fundamental building block of a central processing unit (CPU) in any computing system. Using reversible logic gates instead of traditional logic AND/OR gates, a reversible ALU whose function is the same as traditional ALU is constructed. Programmable reversible logic gates are realized in Verilog HDL, the simulation results have been verified using the QCADesigner. Reversible logic has ability to reduce the power dissipation which is the main requirement in low power digital design. By using the inverse property of reversible logic, all the inputs can be regenerated at the outputs. Thus, by comparing the original inputs with the regenerated inputs, the faults in reversible circuits can be detected. Minimization of the garbage outputs is one of the main goals in reversible logic design and synthesis. The design is based on the reversible multiplexer (RM) synthesized by compact 2:1 QCA multiplexers. The reversible multiplexer is able to achieve 100% fault tolerance in the presence of single missing or additional cell defects in QCA layout. The RALU circuit can be tested for classical unidirectional stuck-at faults using the constant variable used in this design. The experimentation establishes that the proposed RALU outperforms the conventional reversible- ALU's programmability/testability.

Keywords: RTD, SET, TPL, QCA, Verilog HDL, reversible multiplexer (RM), reversible ALU.

I. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) has proposed a few alternative technologies that can replace the transistor based computation in the near future . Some of them are, Resonant Tunneling Diodes (RTD's), Single Electron Tunneling (SET), Quantum Cellular Automata (QCA), Tunneling Phase Logic (TPL), Carbon nano-tubes and Silicon on Insulator (SOI). Among these QCA seems to be the most promising technology that would replace CMOS devices in the near future. Theoretically the idea of cellular automata (CA) was introduced in early 1940s by Von Neumann and Ulam. Later in the year 1993 Lent et al. experimentally demonstrated the possibility of Quantum Dot Cellular Automata cell, with Aluminium Island acting as Quantum dots A quantum dot is a region in the cell structure where charge can localize. A QCA cell consists of _2n' quantum dots with _n' mobile electrons, which can tunnel between the quantum dots of a cell. The compensating positive charge is fixed and immobile. Tunneling out of the cell is completely suppressed due to the potential barriers between the cells. reversibility is the property of circuits in which there is one-to-one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa. Researchers have proved that each bit of information lost will produce KTln2 Joules of heat energy. The energy dissipated due to information destruction will be a significant factor of the overall heat dissipation of the system. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell as illustrated . Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Thus, QCA has no dissipation in signal propagation. Due to high error rates in nano-scale manufacturing, QCA and other nano-technologies target reducing device error.

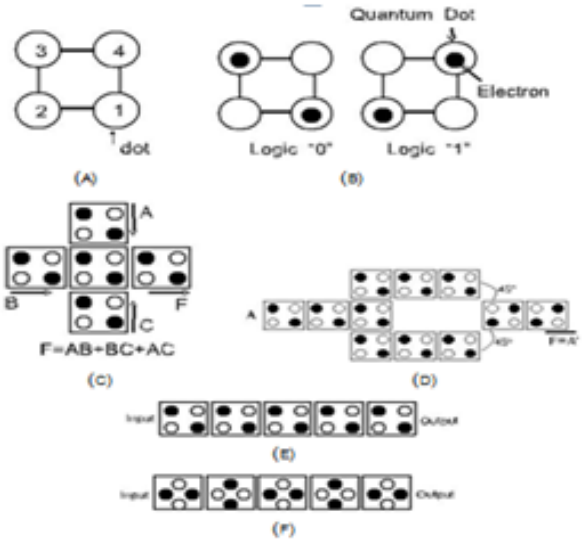

Fig 1: QCA cell and basic QCA Devices. (a) QCA 4 Dots (b) QCA cell as Logic "1"and logic "0", (c)MV,(d) Inverter (INV) , (e) Binary wire, (f) INV chain

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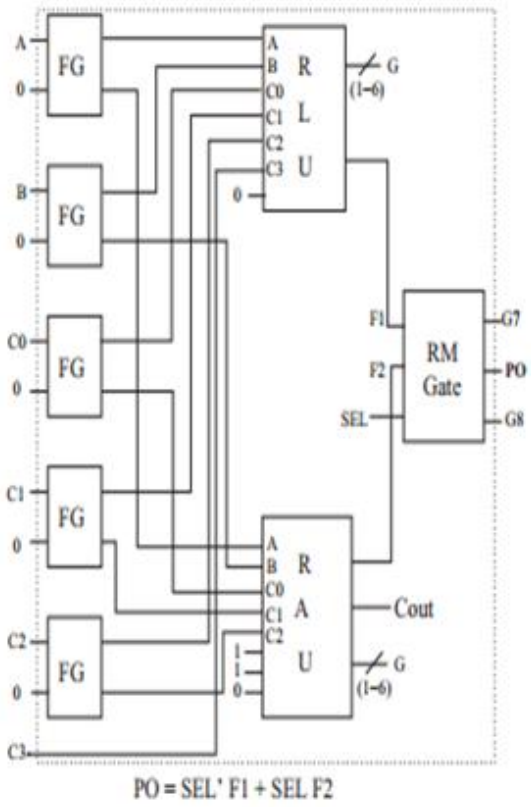
A QCA cell is a coupled dot system in which four dots are at the vertices of a square. The cell has two extra electrons that occupy the diagonals within the cell due to electrostatic repulsion. Fig. 1(a) and (b) shows the four quantum dots in a QCA cell, and the implementation of logic "0" and logic "1" in a QCA cell, respectively. The basic QCA device is the MV or majority gates, which is represented as $F = A\,B + BC + AC$, where F is the majority of the inputs A, B, and C. Another important gate in QCA is the INV. There can be many ways of designing the QCA INV, one of which is shown in Fig. 1(d). In QCA computing, signal transfer is made through wires that are of two types: 1) binary wire and 2) INV chain. The binary wire is shown in Fig. 1(e). The INV chain is shown in Fig. 1(f). In QCA, when a binary wire crosses the INV chain, there is no interaction between the two; hence, the signals in the INV chain and binary wire can pass over each other. In QCA computing, the clock helps in the synchronization of circuits and provides the power required for functionality. QCA clocking consists of four phases: switch, hold, release, and relax.

Our proposed work explores the design of a reversible arithmetic and logic unit (RALU) in QCA Technology. The major contributions of this work revolving around logic based QCA architecture can be summarized in the following points:

- Design of a cost-effective 2:1 multiplexer using QCA followed by its cost effective approach toward least chip-area coverage.
- Synthesis of a reversible structure of 2:1 multiplexer (RM) by compact 2:1 multiplexer.
- Design of reversible logic unit (RLU) and arithmetic unit (RAU) using the proposed reversible multiplexer followed by synthesis of the reversible arithmetic and logic unit with the increase in programmability. The proposed design of RALU is shown to be most efficient on the basis of function generation capability and speed of computation.
- Development of the concurrent testing strategy for detection of any stuck-at fault using only two test vectors.

A. ARCHITECTURE OF REVERSIBLE TESTABLE ALU

The arithmetic logic unit (ALU) is an important constituent of the CPU, as it performs most of the arithmetic and logical operations. It has become an utmost necessity for an effective reversible circuit to increase the depth of programmability of the logic device, i.e. the number of logical calculations produced on the fixed outputs. Also, for a flexible ALU, any modification for implementation in an instruction set architecture should be simple. All of the above factors suggest a modular design methodology, as described in the following subsections. Here, reversible ALU (RALU) is synthesized with two separate modules, a reversible logic unit (RLU) and a reversible arithmetic unit (RAU), based on the RM logic gate. An RM gate enables selection of the output from either the RLU or the RAU.



II . LITERATURE SURVEY

Literature survey enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project. So it is very important part of project.

1.Prameela Kumari. N, K.S.Gurumurthy Presented a paper on, "Quantum Dot Cellular Automata: A Review".

In this paper, survey of various works carried out in the field of QCA with respect to .Materials used in fabricating the quantum dots, Various QCA cell configurations. Clocking mechanism, Basic gate structures, Adder, Multiplier. Divider. ALU. Testing is presented as a first step towards research on QCA and its applications.

2. Himanshu Thapliyal, Nagarajan Ranganathan, Presented a paper on "Design of Testable Reversible Sequential Circuits".

This paper proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed sequential circuits based on conservative logic gates outperform the sequential circuit implemented in classical gates in terms of testability. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit

thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects

3. Himanshu Thapliyal, Nagarajan Ranganathan, Presented a paper "Reversible Logic Based Concurrent error Detection Methodology For Emerging Nanocircuits".

They have demonstrated a new methodology of concurrent error detection in reversible logic circuits. The proposed strategy is based on the inverse property of reversible logic that helps in the regeneration of the inputs. This results in detection of multi-bit errors at the outputs by comparing the original inputs with the regenerated inputs. The inverse and the compare scheme will be able to detect all types of faults in reversible logic circuits. The proposed methodology of concurrent error detection based on property of reversible logic is generic in nature, and will be applicable to any emerging nanotechnology, such as QCA, nano-CMOS designs, which may be susceptible to single or multiple transient and permanent faults. An application of the proposed approach for concurrent error detection in emerging technologies is illustrated for QCA nanotechnology.

4. Kodam. Latha, 2M. Nanda Maharshi, presented a paper ,"DESIGN OF ADDERS USING QCA".

As we dealt with only Adders these are fundamental requirements of logic gates once logic gates are designed we can design all different kind of circuits with QCA-LG the design flow for QCA technology is almost complete. Combinational VHLD/Verilog circuits can be mapped into logic netlists with existing synthesis tools. These netlists can be transformed into QCADesigner compatible layout using QCA-LG, and validated by physical simulation.QCA-LG is still under development. In this paper, they have considered primitives in QCA and have presented an efficient QCA design for an *n*-bit ripple carry adder and various prefix adders. They have also shown that the Brent–Kung adder has lower delay than all other adder designs Further, the Brent–Kung adder performs best among the prefix adders in terms of delay.

5. K K Yadavalli1, A O Orlov, J P Timler, C S Lent and G L Snider, presented the paper "Fanout gate in quantum-dot cellular automata"

This experiment demonstrates the operation of a clocked fanout gate for QCA architecture and makes an important contribution to the family of the functional prototypes of QCA devices. The fanout gate was fabricated in the Al/AlO*x* system and integrates two output latches with an input latch. We demonstrate switching of two electrons in the output latches driven only by one electron in the input latch, made possible by power gain in the output latches. This power gain is seen clearly in the greatly improved signals in the output latches as compared to that in the input latch. In the QCA architecture, the number of output cells driven by a single cell is normally two, a fanout gate. However, since the cells have power gain, they could in principle drive more than two outputs, limited only by the error rate. These extra outputs could be readily added to the existing output latches (to make, for example, a fanout gate with one input driving four outputs). The current implementation features asymmetric coupling between the input and output latches which leads to higher error rate in the operation of the device. Symmetric coupling between the input and the output latches in a more complex device implementation for the QCA fanout gate is proposed which would lead to a reduced error rate in the device operation. The current implementation is only a proof of concept demonstration in the well known Al/Al *x* system. A future fanout gate probably implemented in silicon nanodevices and/or molecular devices could operate at room temperature and with a much reduced error rate.

6. Amit Saxena1, Deepti Shinghal1, Kshitij Shinghal presented a paper on , " Design and Implementation of Adiabatic based Low Power Logic Circuits"

Adiabatic circuits are low power solutions which will soon replace CMOS based logic circuits. From the above results, it is clearly depicted that adiabatic logic circuits reduce power dissipation with a design size penalty in terms of transistor count. Circuit simulations show that with the help of PFAL, the energy savings can be reached at a significant level. Utilizing the basic PFAL technology basic gates (NAND & NOR) are implemented, verified and analyzed. From the simulations the functionality of the implemented logic gates is found to be satisfactory.

7. Mohammad AlFailakawi & Imtiaz Ahmad ,Laila Al-Terkaw presented a paper on "A Greedy algorithm for Low Cost LNN Reversible Circuit Realization".

This paper proposed a greedy algorithm to minimize quantum cost of reversible circuits for Linear Nearest Neighbour realization. The algorithm performance on benchmark circuits was found to reduce quantum cost of the original circuits by approximately 29% for LNN realization. In addition to its simplicity, the greedy algorithm has been recently shown to perform rather compared to more advanced algorithm.

8. Bhuvaneswaran M1, Shankar N.K. presented the paper on , "Efficient Design of MAC Hybrid Adder in Quantum-Dot Cellular Automata".

In this paper, they have presented efficient QCA designs for the Ladner–Fischer prefix adder and a hybridof Ladner–Fischer and the ripple carry adder. The designs are based on new results concerning majority logic.The hybrid

adder is shown to be particularly well suited to the QCA model, it has better performance (in terms of latency) in QCA than a Ladner–Fischer or a ripple carry adder. And also show that the hybrid adder has a smaller area-delay product than existing adder designs in QCA. Area, power are Compared with prior work are presented and the detailed simulation results are also given. The multiplier array, that consist of multiplexers, half adders, full adders and the add cell (to add 0 or 1 to the LSB of the partial products)1. The carry save adder in the adder array is used here as it enables a very fast operation of the adding operation. The accumulator performance can greatly increase the performance of the MAC unit. Shows that the hybrid adder has better performance (in terms of latency) in Quantum-dot cellular automata **(**QCA) than a Ladner–Fischer or a ripple carry adder

9. Akanksha Dixit, Vinod Kapse presented the paper on , "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit".

In this paper, arithmetic, logical unit using reversible control unit has been proposed. they have compared these proposed design with the existing designs in terms of reversible gates used, Garbage outputs, Quantum Cost, Quantum depth, constant inputs, logical & arithmetic functions, and hardware complexity(no. of x-or, and, not gates). Arithmetic & logical unit using reversible control unit has also great improvement over existing designs . It has 10 gate count, 8 garbage output, 29 Quantum cost, 4 constant input which are very less in compare to existing design . And Total 16 arithmetic & logical operations. So the proposed design implementation of reversible ALU in terms of number of gates used, Garbage outputs and Quantum Cost can be used for low power applications. In future we can design complete reversible computer architecture with the help of proposed designs. The reversible ALU will be a central unit in a future design of a fully reversible architecture using only reversible logic elements. For complete architecture, more key elements must be designed including a reversible control unit and a new approach to reversible memory.

10. Premananda B S1, Y M Ravindranath presented paper on, "Design and Synthesis of 16-bit ALU using Reversible Logic Gates".

In this paper they proposed design and synthesis of 16-bit reversible ALU using reversible logic gates instead of conventional gates. The reversibility significantly reduces the use and loss of information bits hence optimal power consumption. The performance checks of various modules are carried out using Cadence tools. Circuits designed using reversible logic showed a reduced power and delay. The discussion has focused on logical reversibility-the inputs and outputs that can be uniquely recovered from each other. Future work one can also try the other aspects of reversible logic-physical reversibility, which is related to the key issue as to whether we can build physical gates and circuits that can actually operate backward and dissipate almost zero power. Still we are facing many challenges before actually turning reversible logic into a practical competitive technology. We are also short of efficient simulation, synthesis, testing and verifying tools for designing reversible logic.

11. Arman Roohi, Hossein Khademolhosseini, Samira Sayedsalehi, Keivan Navi presented the paper on, "A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer".

Multiplexer is an important and fundamental element in most commonly used circuits. This paper presented a novel and efficient design of 2:1 QCA multiplexer. The proposed multiplexer gate and the other suggested gates which are structured by use of it, have been simulated using QCADesigner and tested in terms of complexity (cell count) and area. As it was apparent in simulation results, the proposed multiplexer has some superiority over the previous common designs in QCA and the comparisons evidently showed significant improvements.

12. Debarka Mukhopadhyay , Paramartha Dutta presented the paper on, "Quantum Cellular Automata based Novel Unit 2:1 Multiplexer".

The proposed methodology is an efficient way that greatly reduces no of cells, area and delay in signal propagation from input to output. By this methodology we can go for designing complex multiplexers. This methodology is very simple to implement also. This QCA technology is the future nanotechnology and different classical models can be replaced by this QCA logic and this will become much more efficient and less complex than its classical counterpart.

III. APPLICATIONS

1 . ALU by QCA is the 100% fault tolerant against single bit error & single cell defect, Minimizing the garbage outputs in reversible logic design and synthesis.

2. The total heat generated in the system due to bit loss or information loss can be reduced in reversible testable design.

3. Reversible ALU concurrently tested for multi-bit error at the outputs ,can provide errorless information.

4. Designing of adders using QCA results in better Delay performance compared to conventional adders.

5. The efficient design of online testable multiplexers and de-multiplexers using a novel online testable reversible gate CTSG.

6. Using OTG gate we can design the fast adders, Multiplexer and de Multiplexer. The power dissipation, power utilization, unit time delay and others can be optimized.

IV. CONCLUSION

This work proposes a modular reversible arithmetic logic unit (RALU) which consists of two separate modules – reversible logic (RLU) and reversible arithmetic unit

(RAU). Both the RLU and the RAU are synthesized based on reversible multiplexer (RM) logic introduced in this work having 59% inherent fault tolerance capability in QCA technology. The 100% fault tolerance capability against single missing and additional cell deposition in QCA can be attained by using a fault tolerant structure for few logic primitives inside it. The reversible multiplexer (RM) is synthesized based on three irreversible 2:1 multiplexers proposed in this work. The proposed 2:1 irreversible multiplexer has superiority over the conventional designs available in QCA. The resulting design consists of 19 cells covering an area of only 0.02 μm2, which is substantially lower than the existing ones and uses lesser clock cycles for functioning. The proposed RALU circuits based on reversible multiplexer outperform the ALU circuit implemented with classical gates in terms of testability. The primary advantage of the proposed RALU circuits compared to the conventional ALU circuit is the need of only two test vectors. The decrease in the number of test vectors minimizes the operating expense of test time for a reversible ALU circuit.

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